11 and 12, respectively. Linear gain of 29 dB was obtained with 1.2-W output power at 1-dB gain compression and with 2-W saturation power.

V. Conclusions

A design method for GaAs MESFET power amplifiers has been discussed and a practical method using small signal S_{22} measured at a shallow drain bias condition is presented for the design of output circuits of power FET amplifiers under large-signal operation. Based on this method, a five-stage MIC amplifier with packaged MESFET's was constructed which delivers 1-W power output with 27-dB linear gain and 500-MHz bandwidth in the 12-GHz band. Further improvement of the power performance of the amplifier was investigated using newly developed flip-chip MESFET's. Output power of 4 W is obtained for a balanced unit amplifier and 2 W for a five-stage module.

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Highly Reliable GaAs MESFET's with a Statistic Mean NF_{min} of 0.89 dB and a Standard Deviation of 0.07 dB at 4 GHz

T. SUZUKI, A. NARA, MASAAKI NAKATANI, AND TAKASHI ISHII

***Abstract*—High-performance and high-reliability low-noise GaAs MESFET's are studied from a practical point of view.**

By optimizing the structure and the configuration of GaAs FET's and by developing techniques to form a reproducible thick submicrometer gate, GaAs FET's having improved characteristics have been made.

A mean minimum noise figure NF_{min} of 0.89 dB, a standard deviation of 0.07 dB at 4-GHz CW and a pulse input power capability of more than 0.4 and 2 W, respectively, and a failure rate, supported by field data, of less than 200 FIT have become practical.

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I. Introduction

LOW-NOISE GaAs MESFET's are indispensable for use as microwave amplifiers and oscillators operating in the frequency region over 4 GHz [1]–[3].

Minimum noise figure NF_{min} of 0.6 dB at 4 GHz has been obtained in a laboratory. This value is nearly equal to the value calculated for GaAs FET's with a 0.5-μm gate length [4]. Nevertheless, GaAs FET's with noise figure less than 1 dB at 4 GHz, which are required for low-noise receivers in satellite communication systems, are at present difficult to obtain practically.

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Concerning reliability, mean time to failure (MTTF) of 10^7–10^8 h at 70°C is deduced by thermal acceleration tests [5], [6]. However, as the failure of GaAs FET's in the field is not simply caused by thermal factor, reliability data supported by field tests are, in practice, more important.

In this paper, a study of practical low-noise GaAs FET's having superior performance and high reliability is described. Optimization of the structure and the configuration of device are studied. Devices are characterized with special emphasis of the statistical distribution of noise figure, dc surge pulse capability and RF input power capability. The reliability of improved devices has been examined by field tests.

II. Improvements of GaAs Mesfet's

A. Optimization of Carrier Profile

Since low-noise GaAs MESFET's are operated at drain current as low as 10 to 15 mA under noise-matching conditions, the crystal quality and electrical characteristics of the active layer at the semi-insulating buffer-layer—active-layer interface are very important. The high net carrier density in the active layer and abrupt change of carrier profile are required [7], [8].

GaAs FET's fabricated from three kinds of epitaxial GaAs wafers with different carrier profiles were used. Each was produced by the controlled vapor phase GaAs epitaxial growth technique. Typical results are shown in Fig. 1. The relationship between minimum noise figure NF_{min}, associated gain G_a, and doping profile was also investigated. In the table inserted in Fig. 1, typical NF_{min} and G_a corresponding to the three carrier profiles are summarized. The best results for NF_{min} and G_a are both obtained from profile (B). The higher carrier density of the active region near the buffer layer provides superior performance and the decreased carrier density at the surface provides a higher breakdown voltage between source and gate.

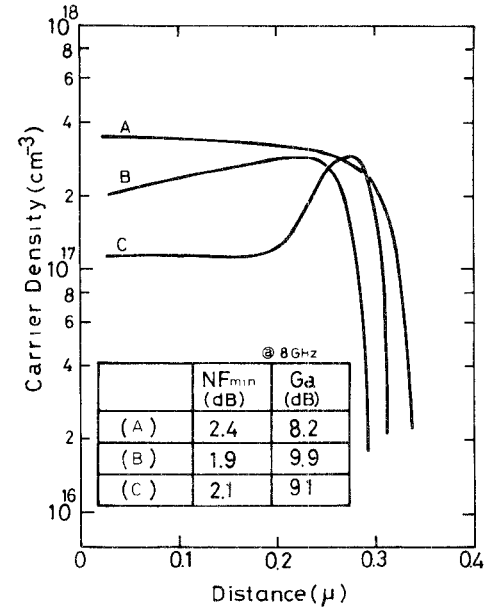


Fig. 1 Carrier profile of three kinds of epitaxial GaAs wafers and typical NF_{min} and G_a values corresponding to these three carrier profiles.

B. Improvements of Structure and Configuration

To improve NF and G_a of GaAs FET's, the reduction of the source-to-gate capacitance C_{gs}, the lowering of the gate to source resistance R_s and the gate series resistance R_g, and the increase of the transconductance g_m [9]–[13] are very important. In Table I, the improvements of the structure and configuration of GaAs FET's for improving these physical factors are shown.

To improve reliability, the design of GaAs FET's should be based on failure analysis. Failure and degradation of GaAs FET's in the field are primarily caused by the accidental application of excess RF input power and dc surge pulse. The modes of failure, gate breakdown, and short circuit between source and drain near the gate pad, caused by thermally initiated process or electrical breakdown, have been observed [14]. Because of it, we therefore, decided to place the gate at position where the gate-to-drain spacing is larger than the gate-to-source spacing to prevent formation of short circuit and to form a gate-recess structure to suppress the concentration of high electric field [15], [16]. R_s increases with increase of the width and depth of the recess, which, therefore, degrades the device performance. The width and depth of the recess should be optimized to balance the improvement of reliability and the degradation of performance.

Considering the above factors, the structure and the configuration of the GaAs FET's are optimized as follows for superior performance and high reliability:

1) narrow and deepen the recess gate portion to minimize the increase of R_s and suppress the concentration of high electric field;
2) use the asymmetric configuration of gate location to lower R_s and to prevent short circuits;
3) use a thick Al submicrometer gate to lower R_g and to obtain increased g_m;
4) use only one gate bonding pad in order to reduce parasitic capacitance and use two fingers to lower R_g and obtain increased g_m.

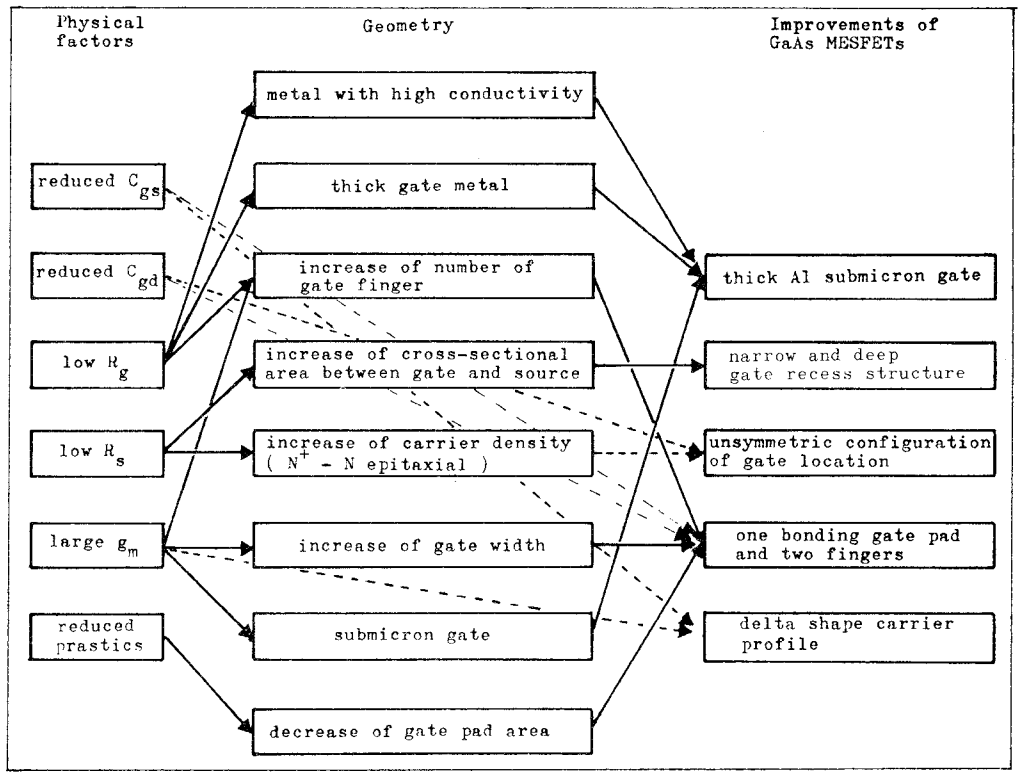
C. Fabrication

The top view and cross-sectional diagram of the resulting GaAs FET's founded on the improvements described are shown in Fig. 2.

The GaAs wafer is constructed from Cr-doped substrate and semi-insulating buffer and sulphur-doped N-type epitaxial layers. The ohmic metal of the source and drain electrodes, with specific sheet resistivity of less than $3\times10^{-7}\ \Omega\cdot cm^2$, was developed by a Au–Ge/Ni metallization system and the source to drain distance is 4 μm. The Al gate with two fingers of 200-μm width, 0.7-μm length, and 0.7-μm thickness was formed by using a practical 1-μm gate photomask.

Formation of the thick submicrometer gate using the 1-μm gate photomask was achieved by the accurate control of the photolithographic process, namely, the thickness of photo resist, the exposure time, the consistence of

TABLE I
IMPROVEMENTS OF GaAs FET'S FOR HIGH PERFORMANCE



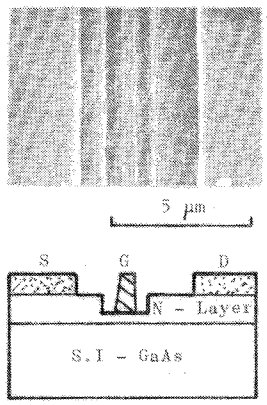


Fig. 2. Top view and cross-sectional diagram of the newly developed GaAs FET's.

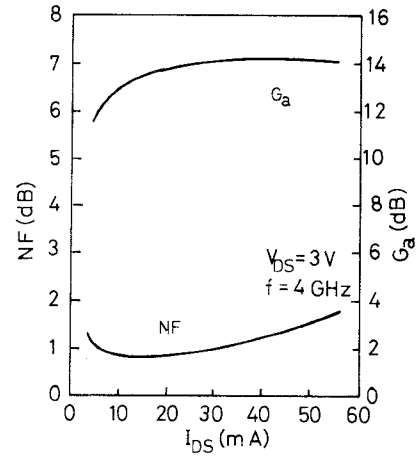


Fig. 3. Typical NF and G_a depending on I_{DS} of GaAs FET's at 4 GHz.

a developer, and the temperature and the time of development. This newly developed technology made the process reproducible and the thick submicrometer gate was formed with high yield. The gate recess with 0.2–0.4-μm depth and 1.0–2.0-μm width is formed using an etchant of $5[CH(OH)COOH]_2 - 1H_2O_2$ of which etching rate is 100 Å/s, at 26.5 °C.

III. Electrical Characteristics and Their Reproducibility

Fig. 3 shows typical NF and G_a as functions of drain current I_{DS} under the conditions of drain to source voltage V_{DS} of 3 V and at frequency of 4 GHz. NF_{min} of 0.9 dB is obtained with G_a of 13 dB at $I_{DS} = 10 - 15$ mA.

Fig. 4 shows the distribution of NF_{min} values for 700 pieces randomly chosen from three lots. The statistic

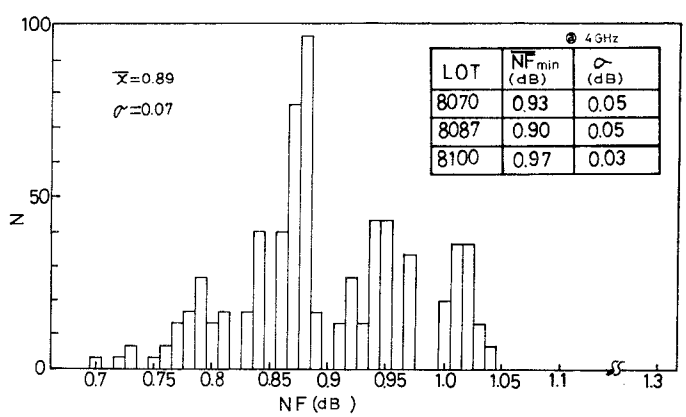


Fig. 4. Distribution of NF_{min} values for 700 devices randomly chosen from three lots.

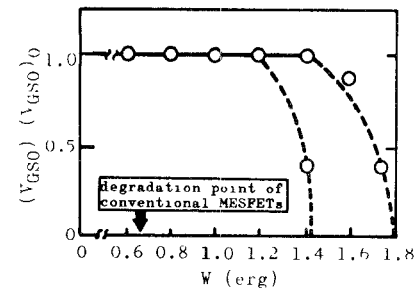


Fig. 5. The dc surge power capability.

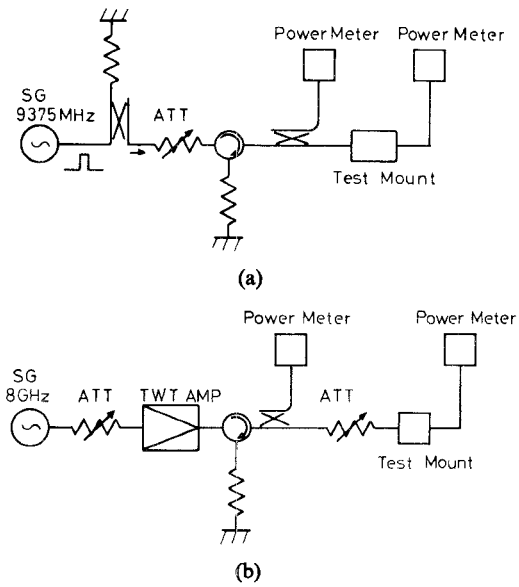


Fig. 6. Test circuit for examining RF input power capability. (a) Test circuit for CW input power capability. (b) Test circuit for pulse input power capability.

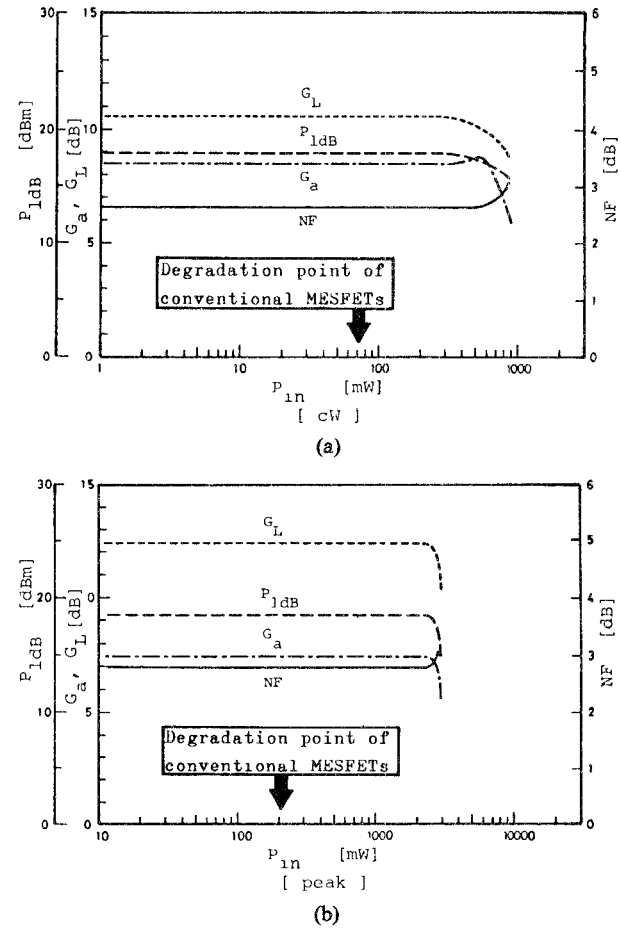


Fig. 7. Power capability of GaAs FET's against CW input power (a) and pulse input power (b).

mean NF_{min} of 0.89 dB is obtained with the standard deviation of 0.07 dB. As the best result, NF_{min} of 0.7 dB was obtained.

From the distribution, 99 percent of the devices provide NF_{min} of less than 1.1 dB at 4 GHz. As shown in the inserted table, the statistic mean NF_{min} and the standard deviation are from 0.9 to 0.97 dB and from 0.03 to 0.05 dB, respectively, for three lots. The newly developed technique to form thick submicrometer gate is confirmed by these results to be practical for use and the structure and configuration for high performance is also confirmed to be optimized.

IV. Reliability

A. Power Capability

Considering that the field failure of GaAs FET's is primarily caused by an accidental large RF power input and dc surge, a high input power capability is indispensable for high reliability. Therefore, the dc surge pulse capability was examined by a condenser discharge method. Fig. 5 shows the change of V_{GSO} for judging the degradation of GaAs FET's against the input energy W. The dc surge pulse capability was assured against energy levels as high as 1.2 erg, a level 2 times higher than those acceptable with conventional devices.

Fig. 6 (a) and (b) show the circuits for examining the pulse and CW power capabilities, respectively. The VSWR's of both test mounts are about 3. In the CW input power capability test, GaAs FET's were biased at $I_{DS}=40$ mA and $V_{DS}=6$ V (gain matching) at a frequency of 8 GHz. After operation for 2 h, the RF parameters of linear gain, G_L, G_a, and NF_{min}, used to judge degradation, were measured.

In the pulse input power capability test, the devices were biased at $I_{DS}=10$ mA and $V_{DS}=3$ V. Pulse power having 1-μs width and 1-kHz repetition rate was supplied at the center frequency of 9375 MHz. The RF parameters of G_L, G_a, and NF_{min} were measured after operation for 10 min.

Fig. 7 (a) and (b) show RF parameter dependency on CW input power and pulse input power, respectively. Degradation was found at about 0.4 W for CW devices as shown in Fig. 7 (a) and at about 2 W for pulsed devices as shown in Fig. 7 (b). These levels were more than 5 times as high as those of conventional GaAs FET's and 10 times as high for pulsed devices.

The power capability depends on the input power condition and on the bias condition. For example, pulse power capability was increased to 2.5 W by addition of a series resistance in the bias circuit and to 3.0 W by addition of a Zener diode in parallel with the bias circuit.

TABLE II
OPERATING RELIABILITY OF GaAs FET'S INSTALLED IN 4-GHz MULTICHANNEL RADIO COMMUNICATION EQUIPMENTS

Representative equipment	4 GHz multichannel radio communication equipment
Operating condition	V_{CC}= 3 V, I_D= 15 - 25 mA
Enviromental condition	Ground, fixed
Number of devices	173
Operating time	11,260 - 28,310 hours
Component hours	2,947,980 hours
Number of failures	0
Failure rate	300 FIT, 60 % confidence level

Confirmed on Sept. 1 1979

B. *Failure Rate Calculated by Field Data*

These GaAs FET's have been used either in low-noise amplifiers under optimized noise matching conditions or in low-power amplifiers under optimized gain matching conditions.

For 173 pieces of GaAs FET's operating in the field, detailed data have been followed up. Results are summarized in Table II. No failure has been observed for 173 pieces of GaAs FET's. The total of component hours is at present 2 947 000 h and the failure rate of 300 FIT is calculated at a 60-percent confidence level. If the laboratory test results are taken into consideration, the failure rate will be less than 200 FIT.

V. CONCLUSION

Optimization of the structure and the configuration of GaAs FET's for high performance and high reliability was studied.

The optimized configuration contained a narrowly and deeply recessed structure, unsymmetric configuration of the gate location, thick submicrometer gate and delta shaped carrier profile.

By developing the technology to reproducibly form thick submicron gates, GaAs FET's with statistic mean NF_{min} of 0.89 dB and standard deviation of 0.07 dB at 4 GHz have become practical.

Concerning reliability, DC surge pulse capability of 1.2 erg was assured, a capability 2 times higher than that for conventional GaAs FET's. RF input power capability of 0.4 W for CW and 2.0 W for pulsed devices could also be guaranteed. These values were more than 5 times higher than conventional values for CW, and 10 times higher for pulsed.

The failure rate less than 200 FIT has become practical.

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